In the Specification:

Please amend the following paragraphs:

[0041] In FIG. 5 a die schematic similar to that of FIG. 1 is shown. Like FIG. 1, the die has sides A, B, C, and D and corresponding pad sites for input, output, input/output, V and G. The functional core logic is connected to the pad sites by leads and input, output, and input/output buffers. FIG. 5 includes additional pad sites A8 and B9 referred to as bypass, and an additional pad site C9 referred to as mode. The mode pad is buffered with leads and an input bufer like a data input. When mode is at a predetermined logic level, say high, the die schematic appears as shown in FIG. 5, and the die is in its functional mode which is exactly the equivalent of the die in FIG. 1. In functional mode, the FCL, input, output, and input/output ~~pads~~ buffers are enabled and the die performs its intended function. In functional mode, the bypass pads are not used.

[0042] In exemplary FIG. 6, the die of FIG. 5 is schematically shown as it would operate in the bypass mode of the present invention. The die is placed in bypass mode by taking the mode pad to a logic state opposite that of the functional mode logic state, in this case a logic low. In bypass mode, the die's FCL, input, output, and input/output buffers are disabled and pad sites of corresponding position between sides A and C and between sides D and B are electrically connected. In bypass mode the die is transformed into a simple interconnect structure between sides A and C and between sides D and B. The interconnect structure includes a plurality of conductors or leads extending parallel to one another between sides A and C, and a further plurality of conductors or leads extending parallel to one another between

sides D and B. While in bypass mode, signals from a tester apparatus can flow through the interconnects between A and C and between D and B to access and test a selected die on a wafer.

[0055] FIG. 16A illustrates an exemplary scheme for performing fault tolerant selection of unsingulated die on wafer. The scheme involves the placement of a small circuit, referred to as a die selector 161, in the scribe lane adjacent each die on the wafer. The die selector 161 shown in FIG. 16B includes an I/O lead or terminal S1, an I/O lead or terminal S2, a mode output lead or terminal, and connections to WV and WG for power. The die selector's mode output is connected to the mode pad of an associated die. The die selectors are connected in series via their S1 and S2 terminals. In the example of FIG. 16A, S1 of the first die selector in the series (at die 1) is connected to PA4, and S2 of the last die selector in the series (at die 64) is connected to PA3. Because the die selector is placed in the scribe lane instead of on the die, the mode pad of the die can be physically probed if required, to override the die selector mode output. This feature permits any die to be tested using the conventional probe testing technique. Because the mode output of the die selector drives only the mode pad of a single die, it can be designed with a relatively weak output drive so that the conventional probe tester can easily override the mode output without any damage to the mode output.

[0062] Exemplary FIGS. 20 and 21 illustrate how to further improve die selector fault tolerance by the addition of a second pair of I/O leads or terminals S3 and S4 in die selector 201. In FIG. 20A, the S3 and S4 serial connection path is shown routed between PA1 and PA2 in the vertical scribe lanes. Separating the S1/S2

(horizontal scribe lanes) and S3/S4 (vertical scribe lanes) routing is not required, and both routings could be in the same horizontal or vertical lanes if desired. It is clear in the example of FIG. 20A that routing S1 and S2 in the horizontal lanes and routing S3 and S4 in the vertical lanes will result in different die selection orders, i.e. S1 and S2 select die order 1, 2, 3 ... 64 or die order 64, 63, 62 ... 1, whereas S3 and S4 select die order 1, 16, 17, ... 64 ... 8 or die order 8, 9, 24 ... 1.